SIR PADAMPAT SINGHANIA UNIVERSITY

Udaipur

SCHOOL OF ENGINEERING

Course Curriculum of 2-Year M.Tech. Degree Programme in Electronics & Communication Engineering (Specialization in VLSI & Embedded Systems) (Batch- 2018-20)

Credit Structure

M.Tech Core		M.Tech Elective	
Category	**Credits**	**Category**	**Credits**
Departmental Core Subjects	48	Departmental Electives	9
Basic Sciences Subjects	3		
Total	51	Total	9
		Grand Total	60

Distribution of Total Credits & Contact Hours in All Semesters

S. No.	Semester Number	Credits/Semester	Contact Hours/week
1	I	15	18
2	II	16	21
3	III	17	22
4	IV	12	18
	Total	60	--

Course Structure: M.Tech. 2018-20

Semester - I

S.No.	Course Code	Course Title	L	T	P	Credit(s)
1	EC-551	Semiconductor Device Modeling	3	0	0	3
2	EC-552	Digital IC Design	3	0	2	5
3	EC-553	VLSI Technology	3	0	0	3
4	EC-554	Digital Signal Processing	3	0	1	4
					Total Credit	15
					Total Contact Hours/week	18

Semester - II

S.No.	Course Code	Course Title	L	T	P	Credit(s)
1	EC-555	Analog Electronic Circuits	3	0	2	5
2	EC-556	Digital System Design using HDL	2	0	2	4
3	EC-557	DSP Architecture & Embedded Systems	3	0	1	4
4	EC-558	MOS Device Modeling	3	0	0	3
					Total Credit	16
					Total Contact Hours/week	21

Semester - III

S.No.	Course Code	Course Title	L	T	P	Credit(s)
1	EC-5XX	Departmental Elective-I	3	0	0	3
2	EC-5XX	Departmental Elective-II	3	0	0	3
3	EC-5XX	Departmental Elective-III	3	0	0	3
4	EC-580A	Dissertation-I	0	0	5	5
5	MA-556	Stochastic Process & Probability	3	0	0	3
					Total Credit	17
					Total Contact Hours/week	22

Semester - IV

S.No.	Course Code	Course Title	L	T	P	Credit(s)
1	EC-580B	Dissertation-II	0	0	9	9
2	EC-580C	Dissertation Viva Voce	0	0	0	3
					Total Credit	12
					Total Contact Hours/week	18

List of Departmental Elective(s) - I

S. No	Course Code	Course Title	L	T	P	C
1	EC-561	System Design	3	0	0	3
2	EC-562	Low Power VLSI Design	3	0	0	3
3	EC-563	Foundations of VLSI CAD	3	0	0	3

List of Departmental Elective(s) - II

S.No	Course Code	Course Title	L	T	P	C
1	EC-564	Artificial Neural Network	3	0	0	3
2	EC-565	VLSI Signal Processing	3	0	0	3
3	EC-566	Machine Learning & Expert Systems	3	0	0	3

List of Departmental Elective(s) - III

S.No	Course Code	Course Title	L	T	P	C
1	EC-567	Active Filter Design	3	0	0	3
2	EC-568	High Speed IC Design	3	0	0	3
3	EC-569	CMOS Mixed Signal Design	3	0	0	3

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Semester - I

(Departmental Core Subject)

EC-551 L-T-P-C
Semiconductor device Modeling 3-0-0-3

Objective: *This course will help the students to acquire a deep & understanding of modeling of FET devices which plays an important role in fabrication of integrated circuits. It should prepare students for research or development of device technology or digital or analog circuits in future.*

Course Content

Concentration & motion of carriers in Semiconductor bulk - Equilibrium concentration in intrinsic & extrinsic semiconductors, Excess carriers, Drift & Diffusion transport, continuity equation. Concentration & motion of carriers at the interface-Surface recombination, surface mobility etc. Device Modeling-Basic equations for device analysis, approximation to these equations for deriving analytical expressions.PN Homojunction-ideal static I-V characteristics & deviations including breakdown, ac small signal equivalent circuit, switching characteristics. MISJunction/capacitor-ideal C-V characteristics & deviations due to interface states/charges & work function differences, threshold voltage. BJT-Transistor action, Static Characteristics, ac small signal equivalent circuit, switching characteristics.FETs-Field effect, types of transistors (JFET, MESFET, MISFET), Staticcharacteristics of MISFET, small signal equivalent circuit, difference between BJT & FETS.

Text/Reference Books

1. Semiconductor Device Modelling With SPICE. Antognetti P. & Massobrio G. 2nd Ed. McGraw Hill. New York. 1993.
2. Advanced Theory of Semiconductor Devices. Hess K. Wiley- IEEE Press.1999.
3. Physics of Semiconductor Devices. 3rd Ed. Sze S. M. John Wiley & Sons. 2007.
4. Physics of Semiconductor Devices. Shur M. PHI.1990.
5. Semiconductor Devices: Modelling & Technology. Das Gupta N. & Das Gupta A. PHI. 2004.

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Semester - I

(Departmental Core Subject)

EC-552 L-T-P-C
Digital IC Design 3-0-2-5

Objective: *This course develops an expertise in full custom, digital integrated circuit design. This course covers several aspects of digital integrated circuit design. Starting with MOSFET equations, it will delve into several areas of digital circuit design, including recent changes in circuit design approaches.*

Course Content

Restoring & non-restoring logic, design & optimization of basic gates, NMOS & CMOS logic design of adders, multipliers, static & dynamic logic, design with overlapping & non overlapping clocks; implementation of state machines using PLAs MACs ALU, shifters, address generators, Memories-Static & dynamic, sense amplifiers. Design rules, stick diagrams, physical layout. Lab: Design, simulation & layout of basic digital blocks.

List of Experiments

1. Design of an Inverter
2. Various types of Analysis of CMOS inverter
3. Designing of NAND & XOR using CMOS logic
4. Designing of Multiplexer circuits using CMOS logic
5. Designing of full adder using CMOS logic
6. Designing of logic circuits using Pseudo NMOS
7. Designing of logic gates using transmission gates

8. Designing of MUX using transmission gates
9. Designing of circuits using Dynamic Logic family
10. Designing of circuits Domino logic families
11. Creating Symbols of circuits
12. LVS for an inverter

Text/Reference Books

1. CMOS Digital Integrated Circuits. Kang L. 3rd Ed. Tata McGraw Hill.2003.
2. CMOS VLSI DESIGN: A Circuits & Systems Perspective. Weste N. & Harris D.M. 4th Ed. Pearson.2011.

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Semester - I

(Departmental Core Subject)

EC-553 L-T-P-C
VLSI Technology 3-0-0-3

Objective: *This course makes the students to understand the basic concepts of VLSI Technology & design of Combinational & Sequential circuits & comprehend the electrical properties of MOS devices & the relation between physical & electrical parameters of MOS device.*

Course Content

MOS structure, Threshold voltage, its correction by body bias & ion implantation. NMOS, PMOS, CMOS. MOS IC technology: Masking steps in metal gate & silicon gate technologies. Basic bipolar IC technology: Masking steps, component isolation techniques, problems of metal cross over. Digital MOS circuits with saturated mode, triode mode & depletion mode loads & CMOS. Static & dynamic performance bR ratio, ratio less logic. MOS Circuit design on the chip for given set of technology parameters & voltages. Effect of tolerances or spreads in VDD, VT, VP, mobility & temperature design. Influence of "body effect" on design. Manufacturer's design rules, Circuit layout in metal gate & silicon gate technologies. Design using Lamda based design rules of Mead & Conway. Pass transistor logic in NMOS & CMOS systems, Mapping from relay logic into silicon to evolve pass transistor logic, pass transistor ALU, tree network, multiplexer-demultiplexer circuits, selector logic, tally circuits, delays in pass

transistor logic, use of level restoring inverters. Driving large capacitive loads, ordinary buffer chain & super buffers. Two phase clocking schemes, gate capacitance as a temporary store & pass transistor shift registers. Register to register transfer, structured design methodology of Mead & Conway.

Use of stick diagrams for design of topology of layout. MOS PLA's, their stick diagrams & layout, finite state machines. Bottom up & top down design. Custom design. Various semicustom design approaches. Choice of technology, I2L logic.

Computer aids for design, logic simulation, circuit simulation, layout, VLSI testing. Problems in going from LSI to VLSI. Scaling for VLSI.

Text/Reference Books

1. Design of Analog CMOS Integrated Circuits. Razavi B. McGraw Hill. 1999.
2. CMOS Analog Circuit Design. Allen P.E. & Holberg D. R. 3rd Ed.Oxford University Press.2012.

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Semester - I

(Departmental Core Subject)

EC-554 L-T-P-C
Digital Signal Processing 3-0-1-4

Objective: *This course is designed to provide students with a comprehensive treatment of the important issues in design, implementation & applications of digital signal processing concepts & algorithms.*

Course Content

Discrete – Tine signals & systems: Basic sequences & sequence operations. Linear time invariant systems Causality & stability. Linear constant coefficient difference equations. Discrete-time Fourier transform & its properties. Convolution & modulation theorems. Complex variables: Contour integrals; Cauchy's integral formula; residues & residue theorem.

Z-Transform: Properties of the region of convergence. Inverse z-transforms.Z-transform properties. Sampling of Continuous-Time Signals: Periodic sampling. Frequency domain representation of sampling. Reconstruction of a band limited signal form its samples. Changing the sampling rate using discrete time processing. Multirate signal processing. Transform Analysis of LTI Systems: Frequency response of LTI systems. Relationship between magnitude & phase. All-pass systems. Minimum phase systems, Generalized linear phase systems. Structures of Discrete-Time Systems: Signal flow graph representation of linear constant coefficient difference equations. Basic IIR structures.Transposed forms.Basic structures for FIR systems.Overview of finite-precision numerical effects. Discrete Fourier representation of finite duration sequences: discrete

Fourier series & its properties. Fourier transform of periodic signals. Sampling the Fourier transform. Fourier representation of finite duration sequences: the discrete Fourier transform & its properties. Circular convolution, linear convolution using DFT.

List of Experiments

1. Linear convolution of two given sequences
2. Circular convolution of two given sequences
3. Computation of N- Point DFT of a given sequence
4. Realization of an FIR filter (any type) to meet given specifications. The input can be a signal from function generator / speech signal
5. Audio applications such as to plot a time & frequency display of microphone plus a cosine using DSP. Read a wav file & match with their respective spectrograms
6. Noise removal: Add noise above 3kHz & then remove; Interference suppression using 400 Hz tone
7. Impulse response of first order & second order system

Text/Reference Books

1. Discrete Rom Signal and Statistical Signal Processing. Therrien W. C.Prentice Hall. 1992.
2. Adaptive Filter Theory. Haykin S. 5th Ed. Pearson Education. 2014.
3. Digital Signal Processing. Salivahanan S. & Vallavraj A. 2nd Ed. Tata McGraw Hill.2001.

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Semester - II

(Departmental Core Subject)

EC-555 L-T-P-C
Analog Electronic Circuits 3-0-2-5

Objective: *The objective of this course is to understand the basic physical structure, principles of operation, electrical characteristics & circuit models of the most important semiconductor devices & to use this knowledge to analyze basic electronic application circuits.*

Course Content

Nonlinear one-port & two-port circuits; Large signal & small signal incremental analysis; Incremental y parameters for obtaining gain; nMOS transistor; Common source amplifier; biasing; ac coupling the signal; Sensitivity to MOS parameters; Biasing a MOS transistor at a givencurrent; Current mirror bias; Drain feedback bias; Source currentbias; Using resistors instead of current sources; Negative feedback amplifiers using operational amplifiers(Op amp); Assigning Opamp signs; Voltage-controlled & current-controlled voltage sources using an Opamp; Controlled sources using atransistor---common drain & common gate amplifiers; pMOS transistor; Converting nMOS transistors to pMOS; Common source amplifier with an active load; CMOS inverter; Biasing in the high gain region Differential pair; Half circuits; Single stage Op amp; Two stage Opamp; High frequency model of a MOS transistor; Common source amplifierfrequency response; Pole splitting; Common drain & common gateamplifier frequency responses; Negative feedback amplifiers with one, two, or more poles in feedback; Loop gain & stability

criteria; Phase margin; Frequencycompensation; Bipolar transistors; Elementary amplifier stages using bipolar transistors.

List of Experiments

1. Performance of DC analysis for an Inverter circuit for evaluation of DC operating point analysis for an inverter circuit & evaluation of the transient analysis for an inverter circuit
2. Performance of AC analysis for an inverter circuit
3. Realization of various logic gates using schematic level & observation of their static characteristics
4. Designing 1-bit full adder using CMOS & find out the power & static characteristics
5. Realization of a 4X1 MUX using transmission gate & observation of the static charac-teristics
6. Designing of various flip-flops using CMOS & observation of the static characteristics
7. Drawingthe layout of a CMOS Inverter gate using MOSIS rules & simulate it
8. Drawingthe layout of a CMOS & gate using MOSIS rules & simulate it
9. Drawingthe layout of a CMOS OR gate using MOSIS rules & simulate it
10. Drawing the layout of a CMOS XOR gate using MOSIS rules & simulate it

Text / Reference Books

1. Microelectronic Circuits. Sedra A. & Smith K. C. 5th Ed. Oxford University Press. 2007.
2. Analog Integrated Circuits. Gray P., Hurst L.P. S. & Meyer R. 5th Ed. John Wiley. 2009.
3. Design of Analog CMOS Integrated Circuits. Razavi B. Tata McGraw Hill. 2002.

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Semester - II

(Departmental Core Subject)

EC-556 L-T-P-C
Digital System Design using HDL 2-0-2-4

Objective: *Students will be able to design & manually optimize complex combinational & sequential digital circuits, Model combinational & sequential digital circuits by HDL, design & model digital circuits with HDL at behavioral, structural, & RTL, levels, develop test benches to simulate combinational & sequential circuits, Perform functional, timing verifications & synthesis of digital circuits & systems.*

Course Content

Introduction: ASIC Design Flow, Introduction to HDL, Language Constructs & Conventions in HDL, Gate Level Modeling, Architecture of FPGA.

Combinational Logic Design: Modeling at Data Flow Level, Continuous Assignment Structures, Delays & Continuous Assignments, Assignment to Vectors, Operators, HDL for combinational Circuits, Design of Adder, Subtractor, Decoders, Encoders, Multiplexer, code Converter.Sequential Logic Design: Behavioral Modeling: Operator & Assignments, Functional Bifurcation, Initial & Always Construct, Assignments with Delays, wait construct, Multiple always blocks, If & if-else, assign-deassign, repeat Construct, Loop Construct: for, while & forever, Parallel blocks, force-release construct, event, Design of Flip flop, Shift register & Counters using HDL.Modeling Techniques: Functions, Tasks, user defined primitives, State Machine: Moore & Mealy state model, HDL code for moore-type FSM, Specification of Mealy FSM using HDL, Mealy-type & Moore-type FSM for Serial Adder.User defined Primitives: UDP Basics, Combinational UDPs, Definition, state

table, & instantiation, Sequential UDPs, Level-sensitive, Edge-sensitive UDPs.Programming Language Interface: Use of PLI,Linking & Invocation of PLI Tasks, International Data Representation, PLI Library Routines, Access Routines, Utility Routine. Current Trends: Latest trends in HDL as Advanced Verification techniques & HDL Simulator.

List of Experiments

1. Designing & verifying through SVL of resistive load common source amplifier & find the transfer characteristics
2. Designing & verifying through SVL of diode connected load common source amplifier & find the transfer characteristics
3. Designing & verifying through SVL of current source load common source amplifier & find the transfer characteristics
4. Designing & verifying through SVL of common gate amplifier & find the transfer characteristics
5. Designing & verifying through SVL of common drain amplifier & find the transfer characteristics
6. Designing & verifying through SVL of differential amplifier & find the transfer characteristics
7. Designing & verifying through SVL of differential to single-ended circuit & find the transfer characteristics
8. Designing & verifying through SVL of basic current mirror & find the transfer characteristics
9. Designing & verifying through SVL of cascode current mirror & find the transfer characteristics
10. Designing & verifying through SVL of voltage mode buffer & find the transfer characteristics

Text / Reference Books:

1. Fundamentals of digital logic with Verilog design. Brown S. & Zvonko V.Tata McGraw Hill.2002.
2. Digital Systems Design using VHDL. Roth H. C. Thomson Publications. 2004.

3. Advanced Digital Design with Verilog HDL. Ciletti M.D.. PHI. 2005.

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Semester - II

(Departmental Core Subject)

EC-557 L-T-P-C
DSP Architecture & Embedded Systems 3-0-1-4

Objective: *This course helps students to understand the basic DFT, FFT & rate conversion algorithms number format, dynamic range & sources of errors in DSP systems & learn about TMS programmable DSPs & their programming capabilities.*

Course Content

Introduction to Digital Signal Processing, Digital Signal Processing Systems, The TMS320 Family, Digital Signal Processing Applications, Digital Signal Processor Architectures: Introduction, CPU Operations, Memory configurations, Peripherals & Input/output, Software Developments, Hardware Issues, System Considerations, using Assembly Programs & Linker-Comms Files, Creating the Project, Building the Project, Debugging the Program, Viewing Memory & Graphics, Using Breakpoints & the Profiler, Fundamentals of Digital Signal Processing: Digital Signal & Operations, The z-Transform, Digital Systems, Frequency Analysis, Random-Signal Processing, A Simple Infinite-Impulse Response filter. Introduction to implantation considerations, data representations & arithmetic: fixed point Numbers & Arithmetic, Floating-Point Arithmetic, Fixed-Point versus Floating-Point Format. Finite- Word length Effects: Input Quantization, Coefficient Quantization, Overflow & Solutions, Coefficient Quantization, Overflow & Solutions, Rounding & Truncation. Programming Issues: Addressing Modes, Concept of Pipelining, Instruction Cache, Hardware & software interrupts, Real-Time Implementation Considerations: Signal Converters, Stream Processing, Block

Processing, Vector Processing, Benchmarks Hardware Interfacing: External Memory Interfacing. Timers & a Master Clock, Serial-Port Interfacing, Timers & a Master Clock, Serial-Port Interfacing, Direct Memory Access Controller, Parallel-Port Interfacing, Host-Port Interfacing, Multiprocessing Techniques, Power-Supply Regulator, Emulator-Interconnect Standard, Fixed-Point Digital Signal Processors: Introduction, TMS320C54X Architecture, Overview & Addressing Modes,TMS320C54X Instruction Set, Programming Considerations & System Issues.

Introduction to Floating - Point Digital Signal, Processors, TMS320C67X: Architecture Issues, Instruction Set, Pipeline Architecture, Programming Considerations, Real Time implementations, Finite Impulse Response Filtering: Definitions, Filter Characteristics, Filter Structures, Filter Designs, Finite Word Length effects, Implementation of Finite - Impulse response Filters, Infinite Impulse response filtering: Definitions, Filter Characteristics, Filter Structures, Stability of Infinite Impulse response filters, Finite Word length effects, Designs & Implementation of Infinite impulse response filters, Introduction to the Discrete Fast Fourier Transform, Fast Fourier Transform Algorithm.

List of Experiments

1. Familiarization with TMS320C6713 DSK
2. Evaluation of aliasing, quantization, data transfers, distortion
3. Evaluation of delays, circular buffers
4. Programming examples for fixed-point DSP
5. Programming examples for floating-point DSP
6. Implementation of finite-impulse response filters
7. Implementation of infinite-impulse response filters

Text/Reference Books

1. Digital Signal Processing. Singh A. & Srinivasan S. Thomson Publications. 2004.
2. DSP Processor Fundamentals, Architectures and Features. Lapsley et al. S. Ch. & Co 2000.
3. Digital Signal Processors, Architecture, Programming and Applications. Venkata Ramani B. & Bhaskar M. Tata McGraw Hill. 2004.
4. Digital Signal Processing. Jonatham S. John Wiley. 2005.

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Semester - II

(Departmental Core Subject)

EC-558 L-T-P-C
MOS Device Modeling 3-0-0-3

Objective: *This course introduces the principles of MOS device modeling wherein MOS device physics & experimentally observed MOS device performance characteristics combined so as to lead to predictable equations & expressions for device performance under various scenarios of excitation*.

Course Content

MOS as 2-terminal device: Ideal MIS diode, Deviation from Ideality. Si-SiO2 system: Oxide Charges. GaAs MIS structure & related problems - Interface Trap Properties from the Capacitance & Conductance-Determination of Flatb & Voltage, Oxide trapped Charges & Radiation effects - Deep levels & DLTS. MOS as 3 & 4- terminal device: Modern MOSFET. Effect of non-uniform doping, Short & narrow channel effects-Threshold voltage shift, subthreshold slope, Velocity saturation, & its effect on transconductance, Hot electrons. Problem of Punch through.SOI MOSFETs.

Text/Reference Books

1. Device Modeling for Analog and RF CMOS Circuit Design. Trond Y., Yuhua C., Fjeldly A. & Wayne W. John Wiley & Sons Ltd. 2003.
2. Solid State Electronic Devices. Streetman B. G & Banarjee S. 5th Ed. Prentice- Hall of India Pvt. Ltd. 2001.
3. Compact MOSFET Models for VLSI Design. Bhattacharyya A. B., John Wiley & Sons Inc. 2009.

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Semester - III

(Departmental Elective - I)

EC-561 L-T-P-C
System Design 3-0-0-3

Objective: *This course provides an introduction to the fundamentals of Computer Aided Design tools for the modeling, design, analysis, test & verification of digital Very Large Scale Integration (VLSI) systems.*

Course Content

Basics of system hardware design. Hierarchical design using top-down & bottom-up methodology, System partitioning techniques, interfacing between system components. multiple clock domains, Synchronous & asynchronous design styles. Interface between synchronous & asynchronous blocks. Meta-stability & techniques. Interfacing linear & digital systems, data conversion circuits.Design of finite state machines, state assignment strategies.Design & optimization of pipelined stages. Use of data flow graphs, Critical path analysis, retiming & scheduling strategies for performance enhancement. Implementation of DSP algorithms. Signal integrity & high speed behavior of interconnects: ringing, cross talk & ground bounce. Layout strategies at IC & board level for local & global signals. Power supply decoupling; Test strategies: Border Scan, Built In Self Test & signature analysis

Text / Reference Books

1. Algorithms and Techniques for VLSILayout Synthesis.Hill D., Shugard D., Fishburn J. & Keutzer K. Academic Publishers. 1989.
2. Application Specific Integrated Circuits. Smith M.J. Addison Wesley. 1997.

3. VLSI Digital Signal Processing. Madisetti V. K. IEEE Press. 1995.

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Semester - III

(Departmental Elective - I)

EC-562 L-T-P-C
Low Power VLSI Design 3-0-0-3

Objective: *This course enables students to identify sources of power in an IC & understand the Power dissipation mechanism in various MOS logic style along with designing of memory circuits with low power dissipation.*

Course Content

Low power CMOS VLSI design: History of low power electronics, sources of power dissipation, degree of freedom, & emerging low power approaches, Power dissipation in CMOS devices: Physics of power dissipation in MOSFET devices, power dissipation in CMOS & its affects, limitations of low power VLSI design circuits, Low power circuits: Modeling for designing in deep submicron technologies, logic circuits & standard cells, low-power very fast dynamic logic circuits, low-power arithmetic operators, circuits techniques for dynamic power reduction, Techniques for leakage reduction:Types of leakage currents in CMOS devices circuit techniques for leakage reduction, low-power & low-voltage communication for SoCs, adiabatic & clock-powered circuits, low voltage design, weak inversion for ultimate low-power logic, robustness of digital circuits at lower voltages, optimizing power at design time ,run time & at stand by, CAD tools for low power VLSI: High-level power estimation & analysis, power macro-models for high-level power estimation & design flow of various EDA companies.

Text / Reference Books

1. Low power CMOS VLSI circuit design. Roy K. & PrasadS.C. Wiley.2000.

2. Designing CMOS Circuits for Low Power. Dimitrios S. Chirstian P. & Costas G.Kluwer. 2002.
3. Low voltage CMOS VLSI Circuits. Kulo J. B. & Lou J.H, Wiley. 1999.
4. Low power digital CMOS design. Chandrasekaran A.P. & Broadersen R.W. Kluwer. 1995.

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Semester - III

(Departmental Elective- I)

EC-563 L-T-P-C
Foundations of VLSI CAD 3-0-0-3

Objective: *This course helps students to understand the concepts behind the VLSI design rules, routing techniques & various algorithms used for floor planning & routing techniques.*

Course Content

Matrices: Linear dependence of vectors, solution of linear equations, bases of vector spaces, orthogonality, complementary orthogonal spaces & solution spaces of linear equations; Graphs: representation of graphs using matrices; Paths, connectedness; circuits, cutsets, trees; Fundamental circuit & cutset matrices; Voltage & current spaces of a directed graph & their complementary orthogonality. Algorithms & data structures: efficient representation of graphs; Elementary graph algorithms involving bfs & dfs trees, such as finding connected & 2- connected components of a graph, the minimum spanning tree, shortest path between a pair of vertices in a graph; Data structures such as stacks, linked lists & queues, binary trees & heaps. Time & space complexity of algorithms.

Text/Reference Books

1. Linear Algebra. HoffmanK. & Kunze R.E. Prentice Hall (India). 1986.
2. Linear Network Theory: Analysis, Properties, Design and Synthesis. Balabanian N. & Bickart T.A. Matrix Publishers Inc. 1981.
3. Algorithms. CormenT., LeisersonC. & RivestR.A. MIT Press & McGraw-Hill. 1990.

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Semester - III

(Departmental Elective - II)

EC-564 L-T-P-C
Artificial Neural Network 3-0-0-3

Objective: *This course provides a clear understanding about the basic neuron models, neural network models, basic learning algorithms & application of artificial neural network*.

Course Content

Introduction: What is a Neural Network, Brain, Artificial Neuron, Classification of Artificial Neural Networks, Architecture of a Neural Network, Activation Functions, Training an Artificial Neural Network, McCulloch-Pitts Neuron Model, Applications of Neural Networks, Comparison of Artificial Neural Networks & Biological Networks, Amari's Learning Rule, HEBB Learning Rule, Delta Rule, Adaline, Madaline System Network, Perception Layer Network, Introduction to Associative Memory, Auto associative Memory, Iterative Auto associative Net, Hetero associative Memory Neural Network, Bidirectional Associative Memory, Storage Capacity, Introduction to Self-Organizing Maps, Fixed Weight Competitive Nets, Kohonen Self-organizing Maps, Counter propagation, Learning Vector Quantization. Back propagation Network: Introduction, Architecture, Algorithm, Choice of Choosing the Various Parameters for a Network Trained by back propagation, Strictly Local Back propagation, Applications of Back propagation Algorithm. Introduction to Adaptive Resonance Network, ART1 Network, ART2 Network, Spatial Temporal Network. Special Networks: Introduction, Probabilistic Networks, Cognitron, Neo cognitron, Optical Neural Networks, Holographic Neural networks. Control Networks: Introduction,

Neurocontroller, Control System Concepts, Control-Problem, System Identification & Control, Adaptive Control Dynamic Systems, Case Study: Inverted Pendulum System.

Text/Reference Books

1. Introduction to Artificial Neural Networks. Sivanandam S. N. & Paulraj M. Vikas Publishing House Pvt. Ltd. 2009.
2. Neural Networks - a Comprehensive Foundation. Haykin S. 2nd Ed. Prentice Hall. 1999.
3. Neural Network Design. Hagan M. T. H. & Beale M.D.. PWS Publishing. 1996.
4. Computational Intelligence Principles, Techniques & Applications. Konar A. Springer. 2005.

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Semester - III

(Departmental Elective- II)

EC-565 L-T-P-C
VLSI Signal Processing 3-0-0-3

Objective: *This course introduces techniques for altering the existing DSP structures to suit VLSI implementations & efficient design of DSP architectures suitable for VLSI.*

Course Content

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound & iteration bound, Longest path Matrix algorithm; Pipelining & parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining & parallel processing for low power, Retiming - definitions & properties; Unfolding – algorithm for Unfolding, properties of unfolding, sample period reduction & parallel processing application; Algorithmic strength reduction in filters & transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters, Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined & parallel recursive & adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining & parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter, Scaling & roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling & roundoff

noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave & asynchronous pipelining-synchronous pipelining & clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low power VLSI chips, charging & discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

Text/Reference Books

1. VLSI Digital Signal Processing systems, Design and implementation. Parhi Keshab K. Wiley Inter Science. 1999.
2. Practical Low Power Digital VLSI Design. Yeap G.K. Kluwer Academic Publishers. 1998.
3. Analog VLSI Signal and Information Processing. Mohammed I. & Fiez T. McGraw-Hill. 1994.

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Semester - III

(Departmental Elective - II)

EC-566 L-T-P-C
Machine Learning & Expert Systems 3-0-0-3

Objective: *This course familiarizes the students with the principle techniques used in implementing machine learning & understand the fundamentals of first generation expert system technology, & the conceptual basis of current attempts to overcome its limitations.*

Course Content

Introduction: Introduction To Knowledge Engineering : The Human Expert & An Artificial Expert – Knowledge Base & Inference Engine – Knowledge Acquisition & Knowledge Representation, Problem Solving: Problem Solving Process: Rule Based Systems – Heuristic Classifications – Constructive Problem Solving, Expert Systems: Tools For Building Expert Systems " Case Based Reasoning – Semantic Of Expert Systems – Modeling Of Uncertain Reasoning – Applications Of Semiotic Theory; Designing For Explanation, Expert System Architecture & Programming: Expert System Architectures, High Level Programming Languages – Logic Programming For Expert Systems, Machine Learning: Machine Learning – Rule Generation & Refinement –Learning Evaluation – Testing & Tuning.

Text/Reference Books

1. Introduction to Expert Systems. Jackson P. 3rd Ed. Pearson Education. 2007.
2. AI and Expert Systems: a comprehensive guide, C language. LevineI., Drang E. & Barry E. 2nd Ed. McGraw Hill. 1990.

3. Artificial Intelligence: A Modern Approach. Stuart R. & Peter N. 2nd Ed. Pearson Education. 2007.
4. Artificial Intelligence & Intelligent Systems. Padhy N.P. 4th Ed. Oxford University Press. 2007.

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Semester - III

(Departmental Elective - III)

EC-567 L-T-P-C
Active Filter Design 3-0-0-3

Objective: *This course helps students to get acquainted with active filter circuits & parameters, design methods & build & investigate active LPF, HPF & BPF.*

Course Content

Operational Amplifier models, Opamp slew rate, Operational Amplifier with Resistive feedback, Analyzing opamp circuits. Examples, First Order Filters: Bilinear transfer function & its parts, realization with passive elements, bode plots, Active realizations, Effect of A(s), Cascade design, Second Order Low Pass & Band Pass Filters: Design parameters Q & w_0, Second order circuit, frequency response of low pass & bandpass circuits, Integrators, Other Biquads, Second Order Filters with Arbitrary transmission zeros: Summing, Voltage feedforward, Cascade design revisited, Low Pass filters with Maximally flat magnitude: Ideal low pass filter, butterworth response, butterworth pole locations, low pass filter specifications, arbitrary transmission zeros, LowPass filters with Equal Ripple Magnitude Response: The chebyshev polynomial, chebyshev magnitude response, local of chebyshev poles, comparison of maximally flat & equal ripple responses. Chebyshev filter design, Frequency. Transformation: Low pass to highpass, low pass to bandpass, low pass to bandstop, lowpass to multiple passband transformation, LC Ladder Filters: Some properties of lossless ladders, a synthesis strategy, General ladder design methods, frequency transformation, design of passive equalizers, Ladder Simulations by Element Replacement: The general impedance

converter, optimal design of the gic, realizing simple ladders, gorski-popiel embedding technique, bruton's fdnr technique, creating negative components

Text/Reference Books

1. Design of Analog Filters. Schaumann R. & Valkenburg V. Oxford University Press. 2001.
2. Integrated Continuous Time Filters. Yannis T. & Johannes V. IEEE Press. 1993.
3. Design of Analog Filters: Passive, Active RC & Switched Capacitor. Schaumann R., Ghausi M.S. & Kenneth L. R. Prentice Hall.1990.

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Semester - III

(Departmental Elective - III)

EC-568 L-T-P-C
High Speed IC Design 3-0-0-3

Objective: *This course identifies the sources which affect the speed of digital circuits & to introduce methods to improve the signal transmission characteristics.*

Course Content

Introduction to high speed digital design: Frequency, time & distance issues in digital VLSI design. Capacitance & inductance effects, high speed properties of logic gates, speed & power. Modeling of wires, geometry & electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines & special transmission lines. Power distribution & Noise:Power supply network, local power regulation, IR drops, area bonding. On-chip bypass capacitors & symbiotic bypass capacitors. Power supply isolation. Noise sources in digital systems, power supply noise, cross talk & inter symbol interference, Signaling convention & circuits: Signaling modes for transmission lines, signalingover lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter & receiver circuits, Timing convention & synchronization: Timing fundamentals, timing properties of clockedstorage elements, signals & events, open loop timing, level sensitive clocking, pipeline timing, closed loop timing, clock distribution, synchronization failure & meta-stability, clock distribution, clock skew & methods to reduce clock skew, controlling crosstalk in clock lines, delay adjustments, clock oscillators & clock jitter PLL & DLL based clock aligners, Clocked &

non clocked Logics: Single-Rail Domino Logic, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families. Latching Strategies: Basic Latch Design & Latching single-ended logic & Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques.

Text/Reference Books

1. Digital Systems Engineering.DallyS. W. & John P. W. Cambridge University Press. 1998.
2. High Speed CMOS Design Styles. BernsteinK. Kluwer.1999.
3. High Speed Digital Design: A Handbook of Black Magic. Howard J. & GrahamM. Prentice Hall PTR. 1993.
4. High Speed Digital Circuits.Masakazu S.Wesley Publishing Company. 1996.

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Semester - III

(Departmental Elective - III)

EC-569 L-T-P-C
CMOS Mixed Signal Design 3-0-0-3

Objective: *This course provides an understanding about the mixed signal circuits like DAC, ADC, PLL etc & obtains knowledge of filter design along with design of different architectures in mixed signal mode.*

Course Content

Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-&-Hold Architectures-Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture, Input/output characteristics of an ideal D/A converter, performance metrics of D/A converter, D/A converter in terms of voltage, current, & charge division or multiplication, switching functions to generate an analog output corresponding to a digital input. Resistor-Ladder architectures, Current steering architectures, Input/output characteristics & quantization error of an A/D converter, performance metrics of pipelined architectures, Successive approximation architectures, interleaved architectures.

Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL -simple PLL, charge-pump PLL, applications of PLL, Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-c integrator, discrete time integrators. Filtering topologies -bilinear transfer function & biquadratic transferfunction.

Text/Reference Books

1. CMOS mixed-signal circuit design. Baker R. J. Wiley India IEEE press.2008.
2. CMOS circuit design, layout and simulation. Baker R. J. Boyce L.PHI. 2000.
3. Design of analog CMOS integrated circuits. Behad R. McGraw-Hill. 2003.

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Semester - III

(Humanities & Basic Sciences Subject)

MA - 556 L-T-P-C
Probability & Stochastic Processes 3-0-0-0

Objective: *The objective of the course is to provide the essential background in random variables & stochastic processes, required to deal with deterministic & probabilistic aspects of communication systems.*

Course Content

Axiomatic definitions of probability; conditional probability, independence & Bayes theorem, continuity property of probabilities, Borel-Cantelli Lemma; random variable: probability distribution, density & mass functions, functions of a random variable; expectation, characteristic & moment-generating functions; Chebyshev, Markov & Chernoff bounds; jointly distributed random variables: joint distribution & density functions, joint moments, conditional distributions & expectations, functions of random variables; random vector- mean vector & covariance matrix, Gaussian random vectors; sequence of random variables: almost sure & mean-square convergences, convergences in probability & in distribution, laws of large numbers, central limit theorem; random process: probabilistic structure of a random process; mean, autocorrelation & auto covariance functions; stationary - strict- sense stationary & wide-sense stationary (WSS) processes: time averages & ergodicity; spectral representation of a real WSS process-power spectral density, cross-power spectral density, linear time-invariant systems with WSS process as an input- time & frequency domain analyses; examples of random processes: white noise, Gaussian, Poisson & Markov processes.

Text/Reference Books

1. Stochastic Processes. Medhi J. 3rd Ed. New Age International. 2009.
2. A First Course in Probability. Ross S. 6th Ed. Pearson Education .2002.
3. An Introduction to Probability Theory andits Applications. Feller W. 3rd Ed. Wiley. 1968.
4. Stochastic Processes. Ross S.M. 2nd Ed. Wiley.1996.
5. Statistical methods (Vol. II). Das N.G. 1st Ed. McGraw-Hill. 2009.
6. Probability statistics and random processes. Veerarajan T. 3rd Ed.Tata McGraw-Hill Education. 2008.
7. Fundamentals of Mathematical Statistics. Gupta S.C. & Kapoor V. K. 11th Ed. S. Chand Sons. 2002.

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Semester - III

(Departmental Core Subject)

EC-580A	L-T-P-C
Dissertation-I	0-0-5-5

The Dissertation for M.Tech. programme consists of two parts: Dissertation-I & Dissertation-II. Dissertation-I is undertaken during the III Semester.

The Dissertation is by far the most important single piece of work in the post-graduate programme. It provides the opportunity for student to demonstrate independence & originality, to plan & organize a large Dissertation over a long period & to put into practice some of the techniques students have been taught in the course. Students will choose a dissertation, in consultation with a faculty member, who will act as the Supervisor.Dissertation involves a combination of sound background research, a solid implementation, or piece of theoretical work, & a thorough evaluation of the dissertation's output in both absolute & relative terms. The very best dissertations invariably covers some new ground, e.g. by developing a complex application which does not already exit, or by enhancing some existing application or method to improve its functionality, performance etc.

The student will prepare the Dissertation report as per the prescribed format/guidelines, & present the same as a seminar at the end of the semester.

The Dissertation will be evaluated continuously over the span of the III Semesters, as per the approved procedure.

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Semester - IV

(Departmental Core Subject)

EC-580B	L-T-P-C
Dissertation-II	0-0-9-9

After completion of Dissertation-I, students will undertake the Dissertation-II in the IV Semester. The idea conceived & progress made in the Dissertation-I shall be extended as Dissertation-II under the supervision of a faculty member. Students shall complete the theoretical & practical aspect of the project. Thereafter they will prepare a report, as per the prescribed format/ guidelines, incorporating the results, their analysis & interpretation. The report, duly certified by the Supervisor, should be submitted to the Head of the Department. The report should also be presented as a seminar at the end of the semester.

Progress made by the student will be continuously monitored throughout the semester & evaluated as per the approved procedure.

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Semester - IV

(Departmental Core Subject)

EC-580C	L-T-P-C
Dissertation Viva Voce	0-0-0-3

Dissertation Viva Voce is the verbal defense of the dissertation carried out by the student in front of a panel of examiners. The objective of Viva Voce examination is to confirm that the piece of work submitted as a dissertation is student's own work, he/she has a sound understanding of the subject of the dissertation, aware of the recent works in the area of dissertation, methodology adopted, & importance/relevance/merits of the output in relation with the existing results in the area.